EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Wen Liu on 05/27/2010.The application has been amended as follows:

As to claim 1, line 8 has been amended as follows, "…drive transistor (14), wherein the device further comprises control circuitry (50) for shifting the amplitudes of the…" and line 10 has been amended as follows, "…conditions, the control circuitry (50) maintaining a constant amplitude difference (39) between the ON gate…".

As to claim 10, line 9 has been amended as follows, "...means (50) for shifting the amplitude of the ON gate voltage and the OFF gate voltage in response to the…" and line 11 has been amended as follows, "…control signal (52), and maintaining a constant amplitude difference between the ON gate voltage and the…".

As to claim 11, line 5 has been amended as follows, "...shifting the amplitude of the ON gate voltage and the OFF gate voltage in dependence on drive and/or…" and line has been amended as follows, "…environmental conditions whilst maintaining a constant amplitude difference between the ON gate voltage...".

As to claim 20, claim 20 has been cancelled.

The following is an examiner's statement of reasons for allowance:

US Patent 7,071,929 to Fujii discloses a display device comprising an array of pixels (Fujii, col. 1, ll. 33-36), each pixel comprising a thin film transistor switching device (14) and a display element (16) (Fujii, col. 1, ll. 33-51), the array being arranged in rows and columns, wherein each row of pixels shares a row conductor (10), which connects to the gates (14a) of the thin film transistors (14) of the pixels in the row (Fujii, col. 1, ll. 33-51), wherein row driver circuitry (30) provides row address signals for controlling the switching of the transistors (14) of the pixels of the row (Fujii, col. 1, ll. 33-51), wherein the row address signals each comprise a waveform (42, 44) for proving an ON gate voltage and an OFF gate voltage to the drive transistor (14) (Fujii, col. 1, ll. 33-51), wherein the device further comprises control circuitry (50) for shifting the ON gate voltage and the OFF gate voltage in dependence on drive and/or environmental conditions (Fujii, col. 7, ll. 24-38, shifting the On gate voltage and the OFF gate voltage period by pulse width modulation), the control circuitry (50) maintaining a constant difference (39) between the ON gate voltage and the OFF gate voltage (Fujii, col. 7, ll. 24-38; col. 4, ll. 35-40); comprising a temperature sensor (54), and wherein the control circuitry (50) shifts the ON gate voltage and the OFF gate voltage in dependence on temperature (Fujii, Abstract); wherein the ON gate voltage and the OFF gate voltage are both higher for lower temperatures than for higher temperatures (Fujii, Abstract); wherein each column of pixels shares a column conductor (12) to which pixel drive signals are provided, and wherein column address circuitry (32) provides the pixel drive signals (Fujii, col. 1, ll. 33-51); comprising a liquid crystal display (Fujii, Abstract);

wherein the control circuitry shifts both of the ON gate voltage and the OFF gate voltage by applying a DC voltage to a common electrode (Fujii, col. 7, ll. 24-54).

US PG Publication 2001/0017611 to Moriyama discloses wherein the control circuitry shifts the ON gate voltage and the OFF gate voltage in dependence on the display device refresh rate (Moriyama, pg. 3, par. 39); wherein the ON gate voltage and the OFF gate voltage are both higher for higher refresh rates than for lower refresh rates (Moriyama, pg. 9, par. 145); wherein there is a portable device having a display device (Moriyama, pg. 1, par. 4).

US PG Publication 2004/0169627 to Hong discloses comprising means for compensating for kickback (Hong, pg. 4, par. 73).

As to claim 1, the prior art of reference fails to teach or suggest *control circuitry (50) for shifting the amplitudes of the ON gate voltage and the OFF gate voltage in dependence on drive and/or environmental conditions, the control circuitry (50) maintaining a constant amplitude difference (39) between the ON gate voltage and the OFF gate voltage.*

As to claim 10, the prior art of record fails to teach or suggest *means (50) for shifting the amplitudes of the ON gate voltage and the OFF gate voltage in response to the control signal (52), and maintaining a constant amplitude difference between the ON gate voltage and the OFF gate voltage.*

As to claim 11, the prior art of record fails to teach or suggest *shifting the amplitudes of the ON gate voltage and the OFF gate voltage in dependence on drive and/or environmental conditions whilst maintaining a constant amplitude difference between the ON gate voltage and the OFF gate voltage.*

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHARLES HICKS whose telephone number is 571-270-7535. The examiner can normally be reached on Monday-Thursday from 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz, can be reached on 572-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal.

Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629